ADDENDUM

TO

SERIES 2073 INTERFACE CONVERTER UNIT

For

IOC202 PLUGGABLE INTERFACE UNIT

June 6th, 2002

A.1 OVERVIEW

The IOC202 PIM accepts one RS-422 signal and produces three TTL output signals. The input signal polarity may be inverted.

The IOC202 uses one Triax input connector, three BNC output connectors, and operates up to 35 Mbps. It drives the Daisy Chain A bus and can be configured to drive the Global A bus as well.

Figure A-1 presents the card panel detail of the IOC202 which details the connector labeling.

A.2 FRONT PANEL CONTROLS AND INDICATORS

The A LED will illuminate whenever there is an active RS-422 IN input. The B LED is not used.

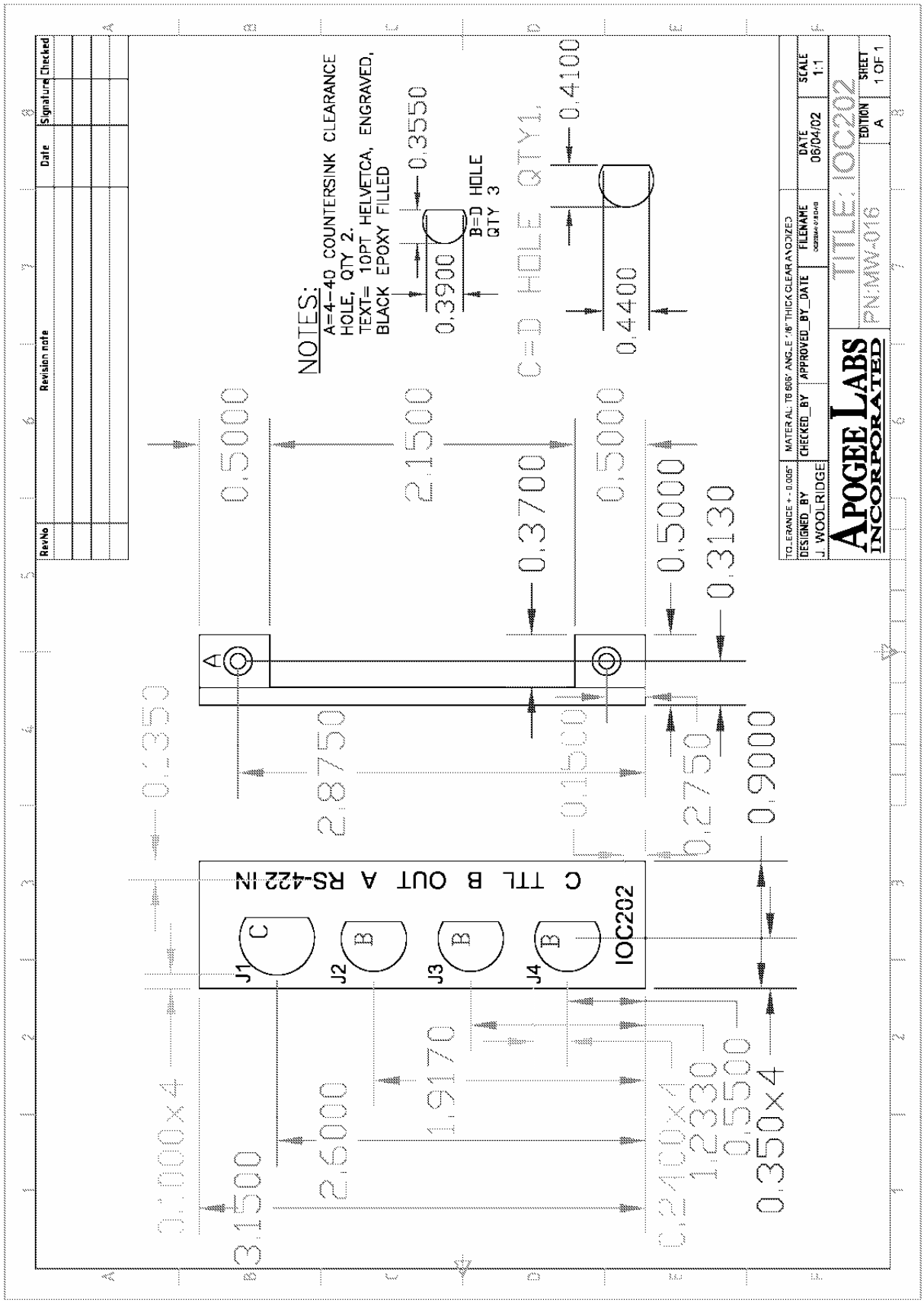
NOTES:
A=4-40 COUNTERSINK CLEARANCE HOLE, QTY 2.
TEXT= 10PT HELVETCA, ENGRAVED, BLACK EPOXY FILLED
B=D HOLE QTY 3
C=D HOLE QTY1.
0.3550
0.3900
0.4100
0.4400
0.5000
2.1500
0.3700
0.5000
0.5000
0.3130
0.3500
2.8750
0.1600
0.2750
0.9000
C TTL B OUT A RS-422 IN
IOC202
J1
J2
J3
J4
0.1000x4
3.1500
2.6000
1.9170
0.2400x4
1.2330
0.0500
0.3500x4
APOGEE LABS INCORPORATED
TITLE: IOC202
PN:MW-016
DESIGNED_BY J.WOOLRIDGE
CHECKED_BY
APPROVED_BY_DATE
FILENAME
DATE 06/04/02
SCALE 1:1
SHEET 1 OF 1
EDITION A

Figure A- 1

A.3 CONFIGURING THE IOC202

Figure A-2 presents the assembly drawing of the IOC202. The following configuration jumpers are provided:

Jumper	Assignment
JP1	RS-422 IN Inversion: 1-2: Invert, 4-5 Not Inverted
JP4	Short to Drive Global bus A
JP5	RS-422 IN Termination: Open: 120Ω Short: 75Ω

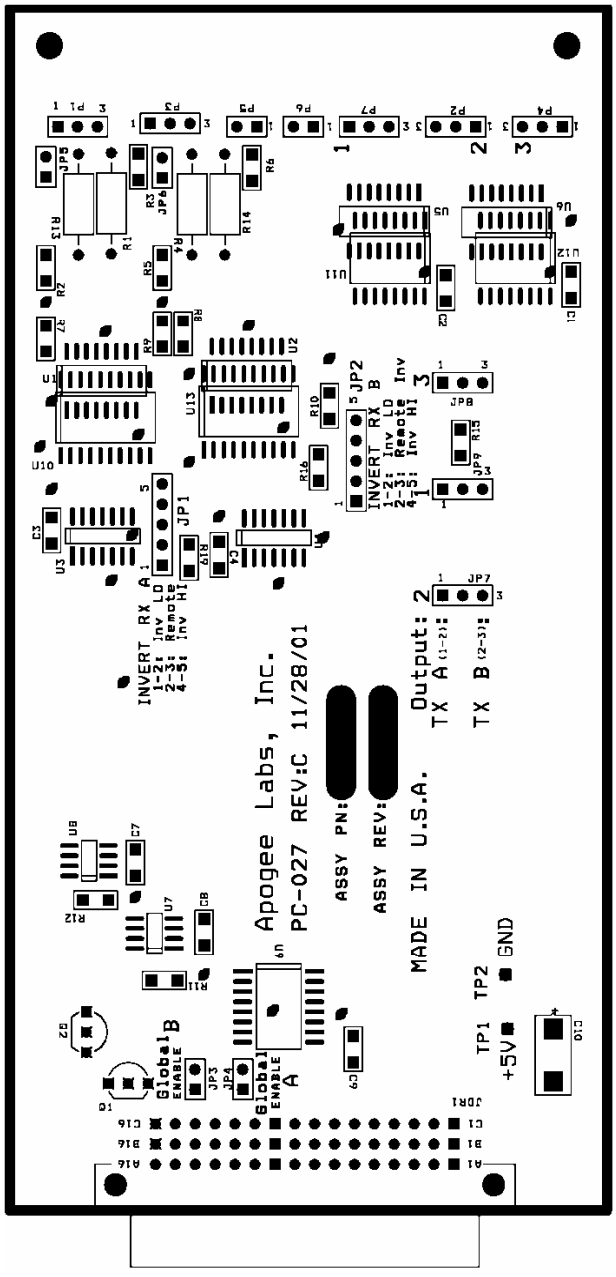

Figure A- 2

A.4 DESIGN OVERVIEW

Refer to the schematics at the end of this addendum for these discussions.

The IOC202 contains one receiver (U1) and two output drivers (U11, U12) for rear panel connection. The Daisy Chain bus A and Global bus A are driven by U9. The Global bus A is enabled by JP4.

U8 controls front panel LED activity. U3 is used for inverting and distributing the input signal.

A.5 DRAWINGS

The following drawings are included:

SHPC-027 Schematic drawings